CHAPTER 1

CIRCUITS

Section 1. Vacuum Tube Basics

1. Introduction

During the 1940s, when the ENIAC was under construction, the basic principles of vacuum tubes and their circuits were familiar to most electrical engineers. Today, however, that knowledge is far less common. For that reason, we begin our discussion of the circuit design of the ENIAC with a brief look at how vacuum tubes work and how they are used as switching elements in circuits. Conversely, the reader is expected to be somewhat familiar with the functions of other circuit components, especially resistors and capacitors.

2. Tube Structure

As the name implies a vacuum tube operates in a vacuum. This allows the electrons (e^-) to flow freely between the electrodes in the tube without being impeded by gas molocules. That vacuum is usually contained in a glass envelope, though sometimes we find them in metal cans. These devices contain at least two electrodes, and those that are used in logic circuits that we study here all have at least three.

a. Cathode. The cathode is the electrode from which the electrons originate. To cause it to give off electrons, its temperature is raised with a heater. In some tubes the heater is the cathode, but for the tubes used in the logic of the ENIAC, the heater is inside a small metal can. This can is coated with a mixture of oxides, such as those of barium and strontium, that efficiently emit electrons at lower temperatures than the heater itself.

b. Plate. The plate (or sometimes anode) is physically designed as a metal can surrounding the cathode with some free space between them. When the plate is at a sufficiently high voltage with respect to the cathode, then the electrons emitted from the cathode travel across the gap between them and hit the plate. When this happens, a current flows through the tube. Note, that the electrons can only flow from the cathode to the plate and not the other way around. A tube containing just a cathode and a plate is called a *diode.*

c. Grid. Tubes can also have one or more grid electrodes between the cathode and the plate. If there is a single grid, then the tube is called a *triode,* if it has two grids, then it is called a *tetrode,* and if it has three grids, it is called a *pentode.* Physically, the grid is usually formed as a wire spiral around the cathode and in the space between it and the plate. The spiral is loose enough

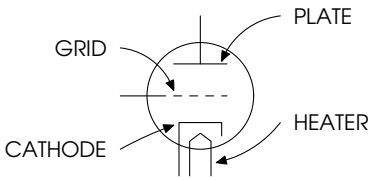

Figure 1. Triode Schematic Symbol

that there is space between the wires for the electrons to pass. If the grid is at the same potential as the cathode, then other than some electrons colliding with the grid wires, it is as if the grid is not there, and current can pass. If the grid is at a negative potential with respect to the grid, then the negative charge around the grid wires repels the electrons as they attempt to travel between the cathode and the plate. This effect prevents current from flowing. In this way, the tube with one or more grids can act as a switch. Figure 1 shows the schematic symbol for a triode with each of the components labeled. Note, that it is common to omit the heater from a diagram, and we will usually do so when describing logic circuits.

3. Simple Tube Circuits

a. Tube Characteristics in Ciruits. When the grid of a tube is sufficiently negative that essentially no current flows, we call this condition *cutoff.* Conversely, when the grid is sufficently positive (at 0 volts or even slightly positive with respect to the cathode), then there is no restriction on the current flow due to the grid. This condition is called *saturation.* When tubes are used for amplifiers, they are typically operated in the region between cutoff and saturation. However, for logic circuits, we want the tubes definitely on or off. So we operate them firmly in cutoff or saturation.

b. When analyzing circuits, we take as a convention that positive current flows from a higher potential to a lower potential. This means that conventional current flows in the opposite direction to the electrons, meaning that the conventional current in a tube flows from plate to cathode.

c. When a tube is operating in saturation, the current flow through the tube implies that there is a very small voltage drop between the plate and the cathode. On the other hand, when the tube is in cutoff, there can be a very large difference in voltage between the plate and cathode. We use this characteristic of the tube extensively in the logic circuits we will examine.

d. Tubes as Simple Switches. In figure 2, we have two simple tube circuits where the tube operates as a simple switch. When considering these circuits, it is important to remember that $V_b > V_c$. We should also point out, that we will generally be assuming that the output of the circuit is fed into a high impedance circuit so that the current flowing throught the ouput is small.

(1) Looking first at the non-inverting circuit (A, fig. 2), if the grid is at a negative voltage, the tube is in cutoff. No current will be flowing through the tube, and the output will be pulled down to V_c through the resistor R_c. If the grid is at a hight voltage level $\geq V_c$, then the tube will be in saturation. Becuase the tube is conducting, the

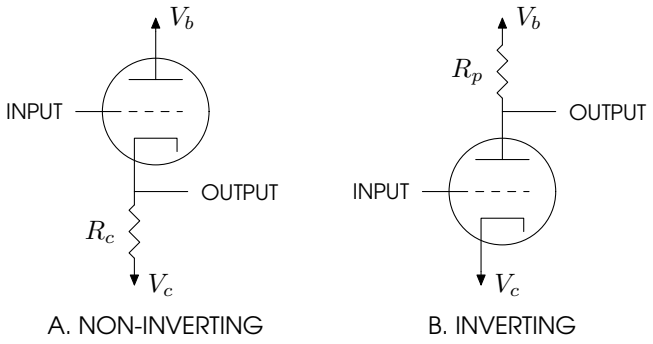

Figure 2. Triode Switching Circuits

voltage difference between the plate and cathode will be small, and nearly all of the voltage dropped between V_b and V_c will be through the resistor R_c. This makes the output close to V_b. Putting it all together, when the input is low ($< V_c$) the output will be low (V_c) and when the input is hight ($\geq V_c$) the output will be high (V_b). A circuit with this configuration is often called a *cathode follower.*

(2) The inverting circuit works in the opposite way. When the input is low, the tube is in cutoff, and no current flows. So the output is pulled up to V_b through resistor R_p. When the input is high, the tube is in saturation, and current flows to reduce the voltage drop across the tube to a small value. This makes the output approximately V_c. The inverting behavior of the circuit is summarized by seeing that a low input leads to a high output, and a high input leads to a low output.

e. Grid Biasing. One problem with the circuits just presented is that they cannot be directly cascaded. That is the output of one can't be used as the input to another. The reason is that the range of voltages that constitute high and low signals for the inputs is different than that which appears on the output. Without getting into the details, we often deal with this by also connecting the grid through a resistor to a voltage source that is negative with respect to the cathode.

Section 2. Boolean Operations

4. General

In modern digital design, we tend to think primarily in terms of signals that are described by expressions using the Boolean operators AND, OR, and NOT. Indeed, we often begin with the Boolean expression and then generate the circuit from that expression, building on the work of Claude Shannon in his influential master's thesis at MIT. However, in the design of the ENIAC, we find a little different design style. Here, we find an approach based around pulses. In the following paragraphs, we see how the set of pulse manipulations in the ENIAC map to Boolean operations.

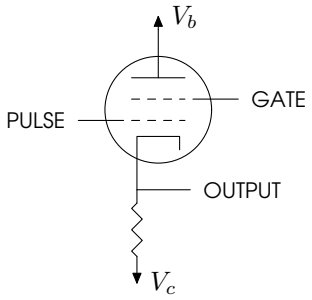

Figure 3. Tetrode Gate (AND) Circuit

5. NOT

In some parts of a circuit, we might need a pulse to be positive-going, but in other parts negative-going. In terms of the high and low logic levels, converting from one to the other is performed by the Boolean NOT. That is the primary use of the inverting circuit we saw earlier. In the contemporary documents written about the ENIAC design, the simple switching circuits are often referred to as non-inverting and inverting *buffers.*

6. AND

As we will see in the larger-scale design of the machine, there a number of places where we wish to selectively allow or disallow a pulse to pass. In the ENIAC this is handled by a *gate.* Whereas today we refer to any of the Boolean logic elements as gates, the gate in the ENIAC always performs an AND function. Typically, the gate is implemented with a single tube having more than one grid. To illustrate this, consider the tetrode circuit shown in figure 3. If we apply the pulse we want to transmit on one grid and the gate signal on the other grid, we get the desired behavior. When either the pulse input or the gate input are low, the corresponding grid is negative with respect to the cathode and the flow of electrons is blocked. However, if the gate input is high when the pulse comes in, then the tube will conduct during the pulse, because both grids are high. When the output is taken from the cathode as shown here, the function of the tube is the same as the Boolean AND. On the other hand, we can get a NAND function, by taking the output from the plate.

7. OR

There are times when we want any of a number of possible pulses to trigger the next stage of the circuit. In effect, we want a Boolean OR. We can achieve this by tying the multiple pulse sources together on a single gate of the tube. This type of function can be realized by the circuit showin in figure 4. Here, the triode shown on top is normally conducting as a result of the pull-up resistor biasing the grid. However, if any of the row of lower triodes is conducting, then its plate pulls the grid of the upper tube down turning the tube off. Thus if all of the inputs are low, their corresponding tubes are off, the pull-up resistor on the output tube turns it on, leading to a low output. On the other hand, if one or more of the inputs are high, then the corresponding input tube is conducting,

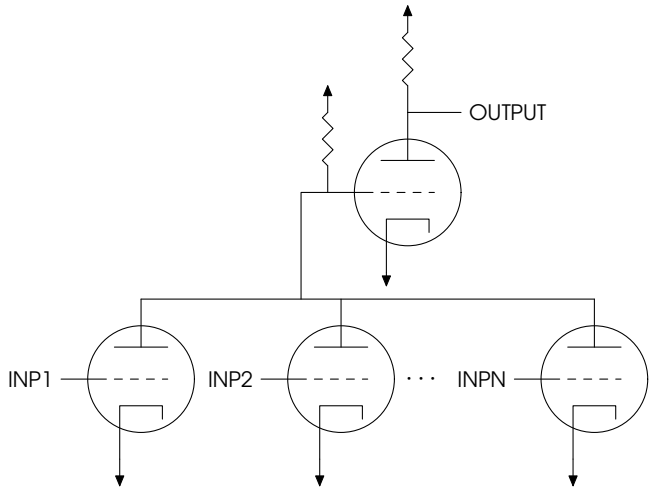

Figure 4. Direct Coupled OR Circuit

pulling the output gate low and turning off the output tube. This results a high output level. This behavior is that of a boolean OR operation.

Section 3. Flip-Flops

8. General

In 1919, William Eccles and F. W. Jordan published a short paper in *The Electrician* describing a circuit for which they had filed a patent the previous year. The paper was titled "A Trigger Relay Utilising Three-Electrode Thermionic Vacuum Tubes." In it, they showed a configuration of cross-connected triodes that had two stable states and could be triggered to switch from one state to the other. This type of circuit is known as a bistable multivibrator, or flip-flop. (It should be pointed out that the term flip-flop was used in a somewhat different way at the time. Here, we use the more recent terminology and take flip-flop to refer to the bistable multivibrator.) By the time the ENIAC was built, collections of flip-flops were being used to build counters and considerable work was being done in a number of labs to improve the speed and reliability of such counters.

9. Basic Flip-Flops

a. General. In the ENIAC, flip-flops are used for a wide variety of purposes. Some of the simpler uses are for remembering events as long as they are relevant. For example, when a signal arrives to initiate a program in one of the units of the machine, it sets a flip-flop that remains set until the program is finished. Similarly, in an accumulator, when the value of a digit transitions from 9 to 0, it sets a carry flip-flop to remember that a carry has occurred and one must be added to the next significant digit. A basic flip-flop circuit suitable for this type of application is shown in figure 5. The tube shown in this figure is a dual triode: that is, two triodes in a single glass envelope. For this circuit,

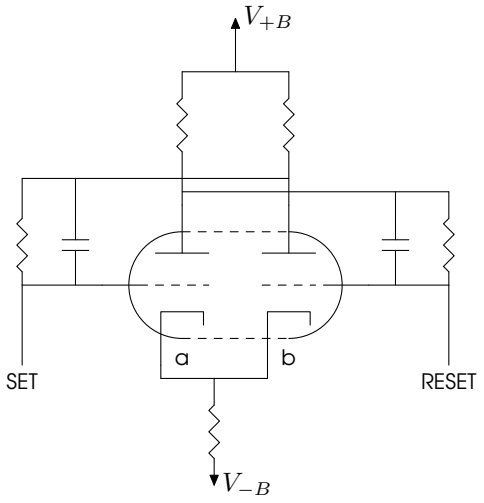

Figure 5. Basic Flip-Flop Circuit

the two stable states are ones where one of the two triodes is conducting and the other is in cutoff.

b. Operation. To understand how the flip-flop operates, let us begin with the circuit in what we will call state I. In this state, the left-hand triode (a) is conducting, and the right-hand triode (b) is off. Because the a plate is at a relatively low potential, the b grid is also held low and keeps the b triode in cutoff. At the same time, the b plate is at a high potential putting a higher voltage on the a grid keeping that triode in saturation. In state II, we have the opposite situation. The a triode is off making it's plate high, making the b grid high turning the b triode on. With the b triode on, its plate is at a lower level, feeding the lower potential to the a grid, keeping it in cutoff.

c. Changing states. In the circuit shown here, the operation we've described assumes that both the SET and RESET inputs are at a low enough voltage to pull the grid of the inactive triode below the cathode voltage. Now suppose that the flip-flop is in state II where triode a is in cuttoff and triode b is conducting. If a positive pulse is placed on the SET input, then triode a will begin to conduct, lowering its plate voltage which reduces the grid voltage on triode b. This causes the plate b voltage to rise reinforcing triode a's conducting state. As this process continues, the flip-flop's state switches to state I. The opposite sequences of events takes places when the circuit is in state I and a positive pulse is received on the RESET input.

d. Flip-flop outputs. Output taken from the plate of triode a is identified as the + output, and that from the b plate as the − output. Since in state I, triode a is conducting, its plate is at a lower voltage than b's plate. Conversely, in state II, plate b is at the higher voltage. Thus the SET input causes the flip-flop to a state where the + output is positive with respect to the − output, and the RESET input causes the − output to be positive with respect to the + output.

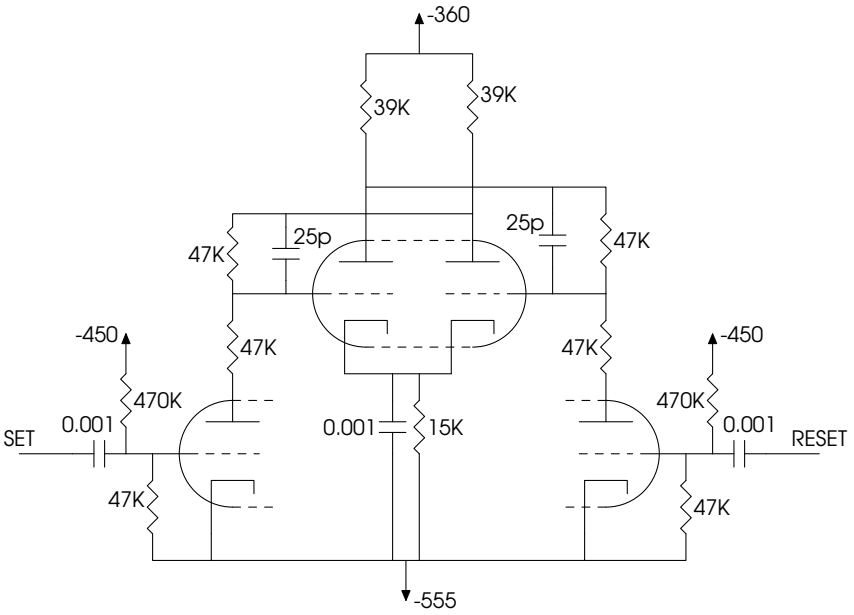

Figure 6. Typical Flip-Flop Usage

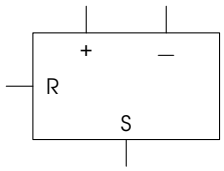

Figure 7. ENIAC Flip-Flop Symbol

e. Driving the inputs. In most instances of this type of flip-flop, a standard design is used to provide the proper levels for the SET and RESET inputs. This circuit is shown in figure 6. Here, the grids on the lower dual triode are biased so that the triodes are normally conducting. This results in the negative bias on the flip-flop grids. When the signal on the SET input transitions from high to low, a negative pulse passes through the capacitor momentarily turning off the associated triode. This causes its plate voltage to pulse high which provides the input to the flip-flop necessary to transition from state II to state I. In the ENIAC drawings a flip-flop of this type is often denoted by the symbol shown in figure 7. The operation of this type of flip-flop is simulated as part of the receiver simulation shown in figure 15.

10. Flip-Flops in Large Counters

a. General. After extensive experimentation and study of several different flip-flop and counter designs, the ENIAC team selected a couple of design approaches to use. The first of these is shown in figure 8 (redrawn from figure 3 in the ENIAC report "Vacuum Tube Counter Circuit (Two Triodes Per Stage)").

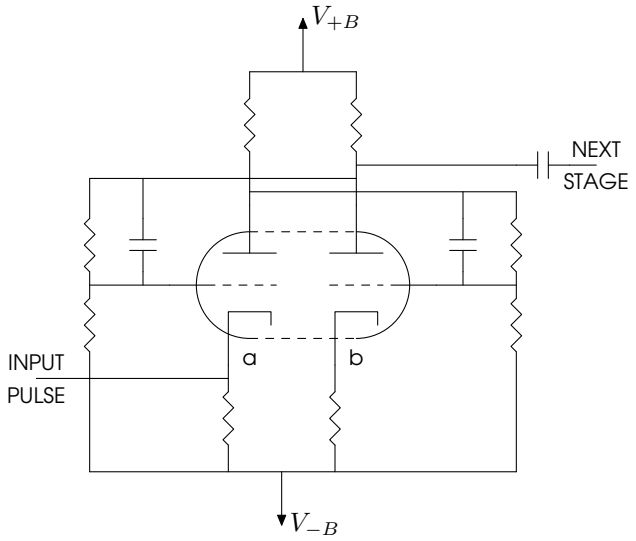

Figure 8. Flip-Flop Used in Multi-Stage Counters

Except for those on the cathodes, the resistors are all of roughly equal values. Those on the cathodes are smaller resistance values. The basic operation of this flip-flop is much like that described in the previous paragraph. The signal in the diagram labeled "NEXT STAGE" connects to the grid of the b triode (the RESET input). A ring counter is formed by a series of these flip-flops connect in a circle so that the first stage becomes the next stage of the last one. In such a counter, all of the stages but one are in state I. Which stage is in state I identifies the value currently stored in the counter.

b. Operation. Now, consider what happens when a negative pulse is put on all the a cathodes simultaneously. For those stages in state I, the cathode is already equal to or negative with respect to the grid, so making it more negative won't change anything. The single stage that is in state II, however, has it's cathode positive with respect to the grid. If the negative pulse on the cathode is sufficient to lower the cathode to less than the grid, the a triode will begin to conduct. This will lower the voltage on the a plate which will then turn off the b triode, switching the stage to state I. When the b triode switches, its plate moves from a lower potential to a higher one. This causes a positive pulse to go through the capacitor connecting it to the next stage of the counter. This next stage is in state I where the b grid is low keeping its triode in cutoff. However, when the positive pulse is applied to the b grid, it causes the b triode to conduct, lowering the b plate voltage. This in turn turns off the a triode in that stage. The net effect of all this is that a negative pulse on the input line connected to all the a cathodes moves the state II condition from one stage to the next in line. This behavior is illustrated by the SPICE simulation shown in figure 9. The trace labeled v(1) is the input to the pulse standardizer (described later), and each of the other traces is the signal on the b triode plate on one stage of a decade counter.

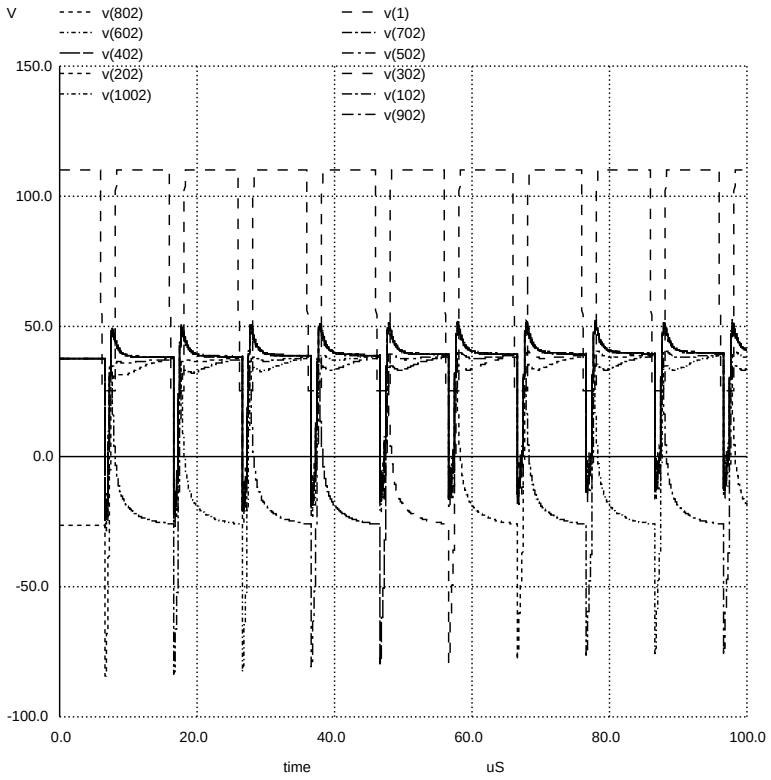

Figure 9. Decade Counter Simulation

11. Two Stage Counter

a. General. In the previous circuits, we have seen the flip-flop toggled by application of a signal to the grid and by application of the signal to the cathodes. The flip-flop state can also be changed by applying a signal to the plate, and this is the technique used for the plus-minus sign (PM) counter in accumulators. The flip-flops used for larger counters use two triodes per stage. Since the sign counter is essentially a two-stage counter, using the same design would suggest four triodes. However, because a single flip-flop gives us two states, we really only need two triodes. At the same time, as with the circuit shown in figure 6, there is an additional triode pair that drives the flip-flop. The circuit used for the PM counter is shown in figure 10.

b. Operation. To understand the operation of this circuit, we start with a positive signal on the CLEAR line. If the flip-flop is already in state I (triode a conducting and triode b in cutoff), then the clear signal has no effect. However, if it is in state II, then the positive pulse on the grid of triode a will cause it to flip to state I as described earlier. Now consider what happens when an input pulse arrives while the counter is in state I. The positive pulse turns on both triodes in the left-hand tube. Becuase, the plates of these triodes are connected

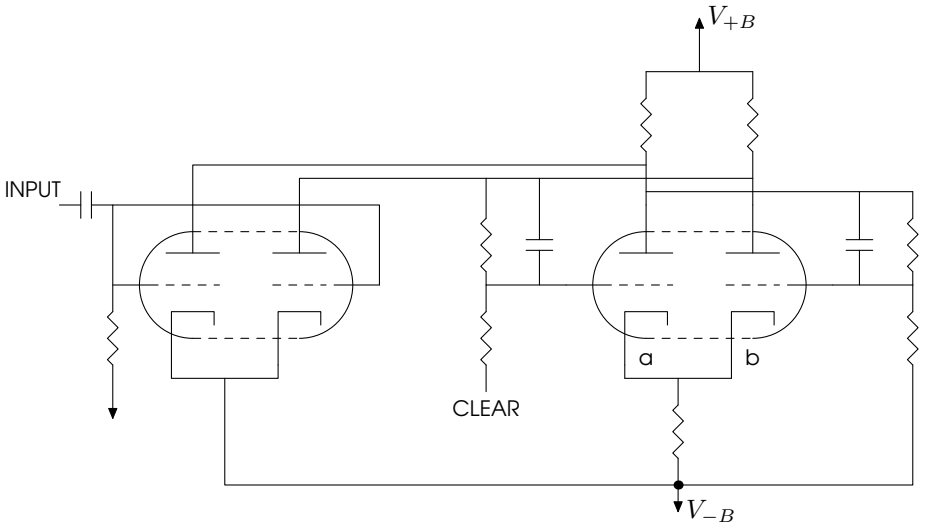

Figure 10. PM Flip-Flop

to those in the other tube, the input pulse pulls all four plates low. Since the circuit is in state I and plate a is already low, the input pulse has relatively little effect on it. The drop in voltage on plate b causes a negative signal to grid a. This initiates the toggling process as in the cases we've already discussed. The same process operates in reverse if the flip-flop is in state II when the input pulse arrives. Figure 11 shows the result of a SPICE simulation of the PM flip-flop driven by a pulse standardizer discussed later in this chapter. The simulation begins with a clear operation followed by three input pulses. In this figure, v(2) is the trace of the input signal, v(19) is the plate of triode a, and v(20) is the plate of triode b.

Section 4. Other Circuits

12. Pulse Standardizer

a. General. Several of the flip-flop designs we've examined are quite sensitive to the shape of the input pulse. In addition, the inter-unit pulses in the ENIAC can travel tens of feet, causing them to be significantly distorted by the capacitance and inductance found in the connecting cables. These two factors lead to the use of circuits that reform the pulses when they enter a unit. This circuit, called a pulse standardizer, is shown in figure 12. The dual triode is a 6SN7 and the other tube is a 6V6. (In reality, the 6V6 is a pentode, but internally, the supressor grid is connected to the cathode. Since there are only four external electrodes, we draw it as a tetrode.) In many cases, such as the accumulator decade counter or the accumulator repeater, the 6V6 is followed by a 6L6 inverter to drive the cathodes of the counters.

b. Operation. This circuit is essentially composed of two parts. The first part is the circuit containing the 6NS7 dual triode. These triodes are connected as a pair of inverters. By using the cutoff and saturation properties of the

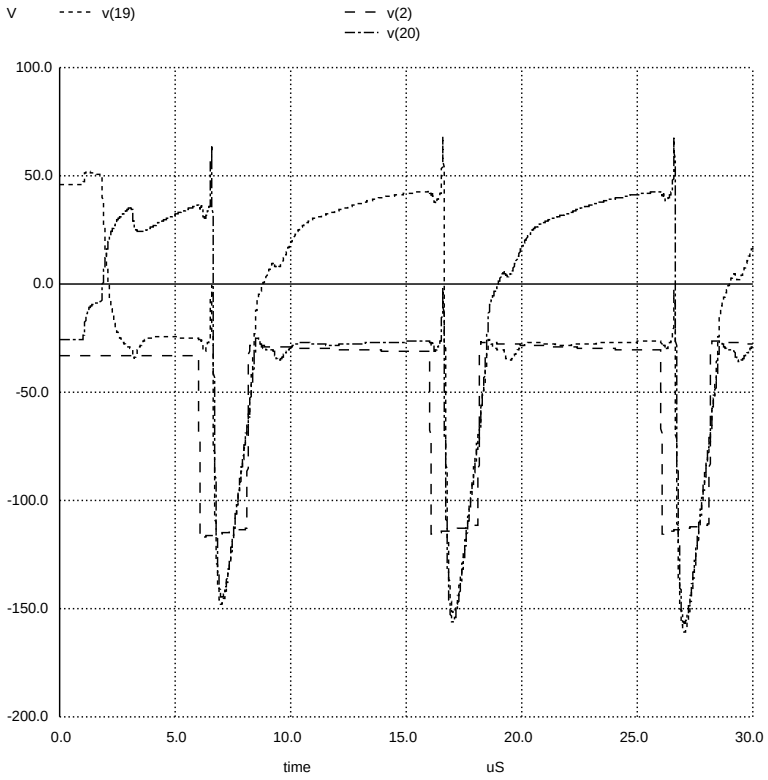

Figure 11. SPICE Simulation of PM Flip-Flop

tubes, this part of the circuit takes a signal that may have been highly distorted into a more square shape. The importance of this is to produce a more sharp rise in the leading edge of the pulse. That signal feeds into the second part of the circuit built around the 6V6 tube. The inductor and capacitor in the plate circuit of that tube produce a carefully shaped pulse. Early research led a design where the rise time of the pulse is 0.25μs and the decay time is 2μs. Figure 13 shows the results of a SPICE simulation of this circuit. The trace labeled v(16) is the output of the circuit feeding a resistive load of 10KΩ.

13. Transmitter

When signals are being transmitted from one unit to another, they travel over potentially long transmission lines. To drive these transmission lines and the impedances they present, a pair of high-power tubes connected in a parallel cathode-follower circuit are used. This pair of 6L6s is, in turn, driven by a 6V6, as shown in figure 14. The 220Ω resistor shown in the output circuit is contained in a load box that is plugged into the end of the trunk of 11 transmission lines. Figure 15 shows the results of a SPICE simulation of the transmitter circuit, where v(5) is the input to the circuit and v(10) is the voltage across the load resistor, ignoring transmission line effects.

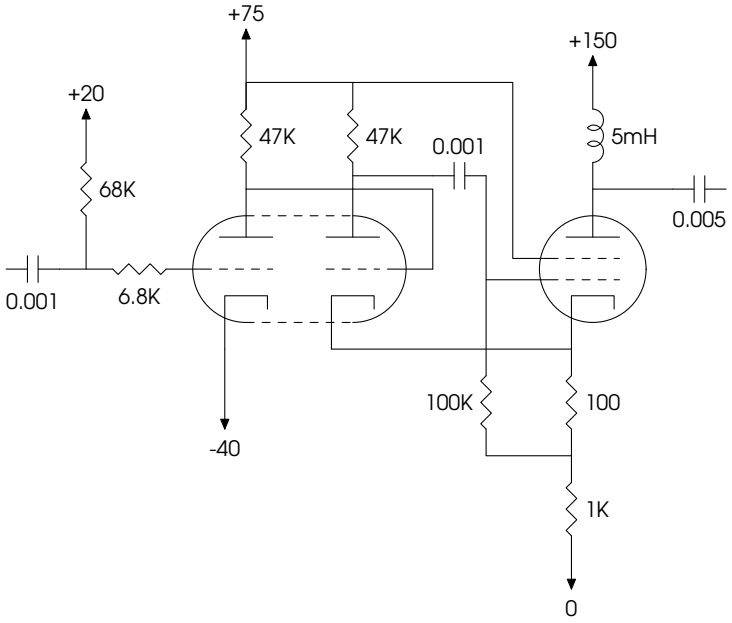

Figure 12. ENIAC Pulse Standardizer

Section 5. Modules

14. Receiver

The next circuit we examine is the receiver. These circuits are the control inputs on various units of the ENIAC. Connected to a transmission line of a control trunk, the receiver gets a pulse sent by a transmitter and latches it into a flip-flop. The flip-flop is reset when the program triggered by the input control signal is completed. The standard receiver circuit can be found in ENIAC drawings PX-1-105, PX-5-115, PX-5-148, and figure 16 here. Drawing PX-5-148 shows that two receivers are included in a single receiver plug-in chassis.

a. Operation. The core of the receiver circuit is the same flip-flop structure shown in figure 6. In the case of the receiver, the operation is best thought of with the set input on the right and the reset input on the left. The right-hand input is driven by a program input line, typically on the unit front panel and connected to a control trunk. Positive control pulses pass through the inverter shown in the lower right of the drawing to provide the negative pulse to the flip-flop input necessary to flip it to the set condition. The input on the left is also diven by an inverter, but one with a gate (a NAND). The two inputs are a reset signal and the state of the flip-flop. A negative pulse is provided to the left-hand flip-flop input only when a reset signal is received while the flip-flop is in the state set by the right-hand input.

b. Timing. Figure 17 shows the results of a SPICE simulation of the circuit in figure 16. There are several important aspects of the timing of controls that are shown in this simulation. First, program input controls are most often

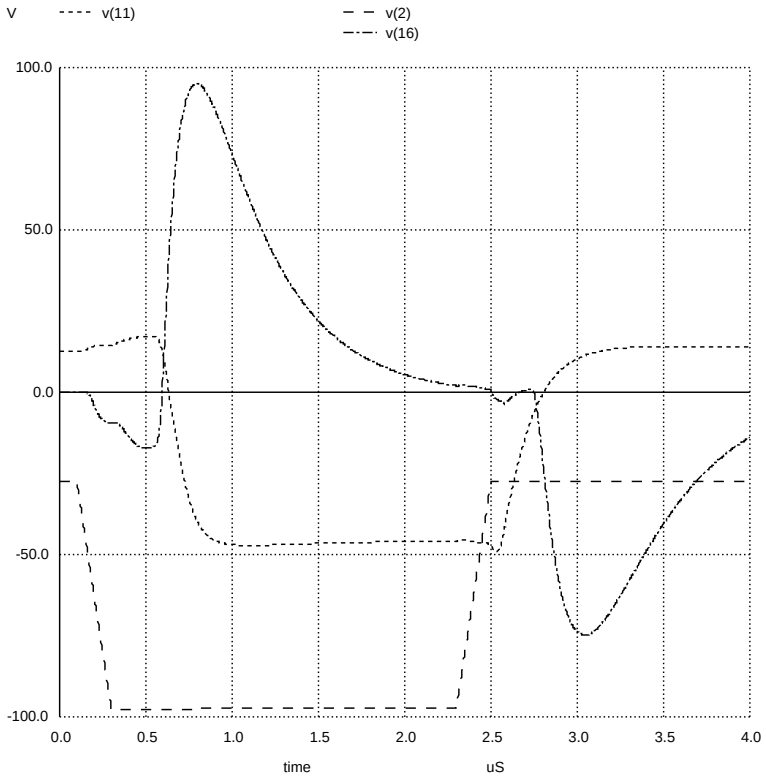

Figure 13. SPICE Simulation of Pulse Standardizer

generated by units as part of their handling of the Central Programming Pulse (CPP). The reset signal for the receiver is generated internally by the unit and is also part of handling the CPP. In figure 17, the signal labeled v(23) is the program input, and the one labeled v(1) is reset. At the beginning of the simulation, these two signals overlap as would typically happen when a program is initiated. Note that because the input to grid 3 of the gate tube (v(7)−v(6) in the graph) is still low, the CPP is not passed to the reset input of the flip-flop. Between 1μs and 2μs later, the flip-flop changes state, roughly coincident with the end of the input pulse. At 50μs into the simulation, another CPP is received. (The cycling unit actually generates a CPP every 200μs, but for the purposes of making the graph easier to read, the interval was reduced to 50μs for this simulation.) This time, the voltage across the 300pF capacitor connected to grid 3 of the gate has increased to the point where the CPP is passed through to the reset input of the flip-flop, returning it to its original state.

c. Outputs. The cross-connected plates of the flip-flop also drive the output circuits of the receiver. In the upper-right of figure 16, there is a triode inverter driving a tetrode cathode follower. The tetrode's cathode is typically connected

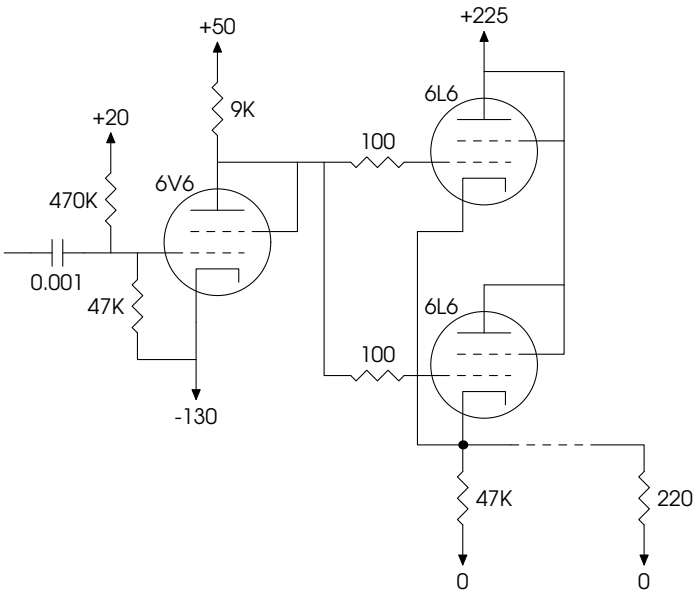

Figure 14. ENIAC Transmitter

to an operation selection switch which then drives the internal controls of the unit. For example, in the accumulator, the operation switch provides the gate signals for routing one of the data input terminals to the decade counters.

d. Programming. As illustrated in this simulation, the RC circuit connecting the right-hand flip-flop plate to grid 3 of the gate prevents a reset from occuring if the flip-flop was not previously set. This means that the programmer need not take any special action when using a pulse that overlaps the CPP to activate a program. However, if a pulse that is not timed by the CPP is used to initiate a program, it can be problematic. As soon as the flip-flop is set, the outputs become active, causing the program to be active during the remaining part of the addition time. Furthermore, if the input pulse occurs more than about 40μs before the CPP, then the CPP will cause the receiver to be reset in the same addition time when it was set. The net effect of this is that receivers should triggered by input pulses that are generated by the CPP.

15. Repeater

When an accumulator program is initiated on any of inputs 5--12, a counter must be activated to control the number of repetitions of that program. The module containing that counter is called a repeater, and its schematic is found in ENIAC drawing PX-5-149. It contains 12 envelopes, of which nine are 6SN7s making up a nine stage ring counter. Each stage of the counter is that shown in figure 8. The remaining three envelopes are the 6SN7, the 6V6, and the 6L6 which make up a pulse standardizer followed by a driver for the counter cathodes. In addition to the power supply connections, the module has two inputs signals, one for advancing the counter and one for clearing the counter.

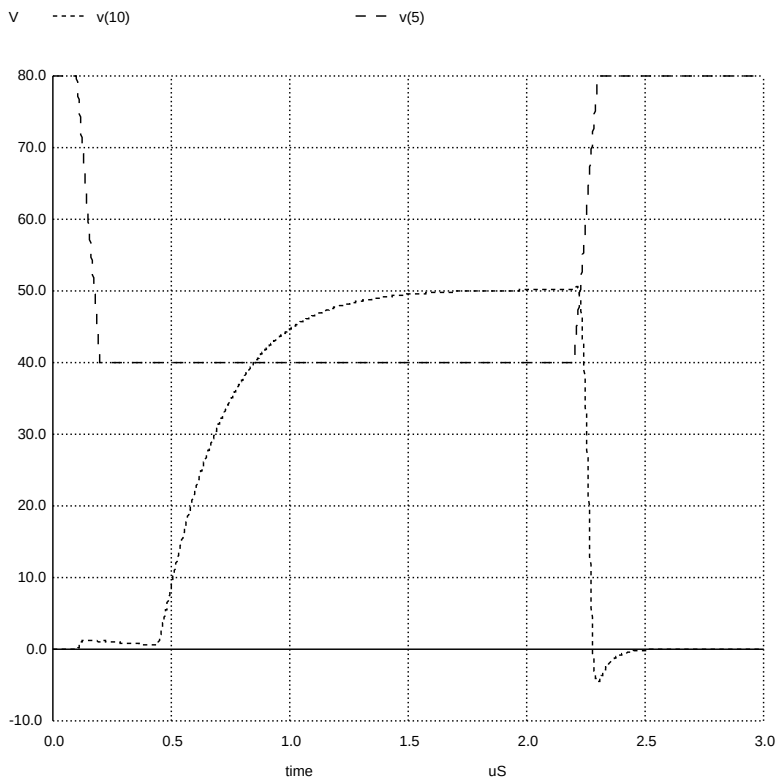

Figure 15. SPICE Simulation of Transmitter

The states of each of the nine counter flip-flops are brought out as outputs of the module. These outputs are connected to the nine poles of a nine-position rotary switch on each of the program controls. We can then take the rotor connection and use it when we need a signal that is active exactly when the repeater is in the stage selected by the switch setting.

16. Transceiver

The program inputs 5--12 are handled by tranceiver modules, rather than receivers. Drawing PX-5-147 shows the schematic of the tranceiver module. The module contains 12 envelopes implementing a single transceiver. The heart of the transceiver is basically the same as the receiver. Figure 18 shows a block diagram of the transceiver module.

a. The first difference between the receiver and the transceiver is found in the reset circuit. Instead of a single gate, the transceiver uses a pair of AND gates. The first of these is called the *repeat coincicence gate* and ANDs the flip-flop state with the signal from the rotor on the repeat switch. Becuase it is in an inverting configuration, this gate's output is low when the program on this transceiver is active and the repeater is in the stage selected by the repeat count switch. It is inverted and used for several output controls described in

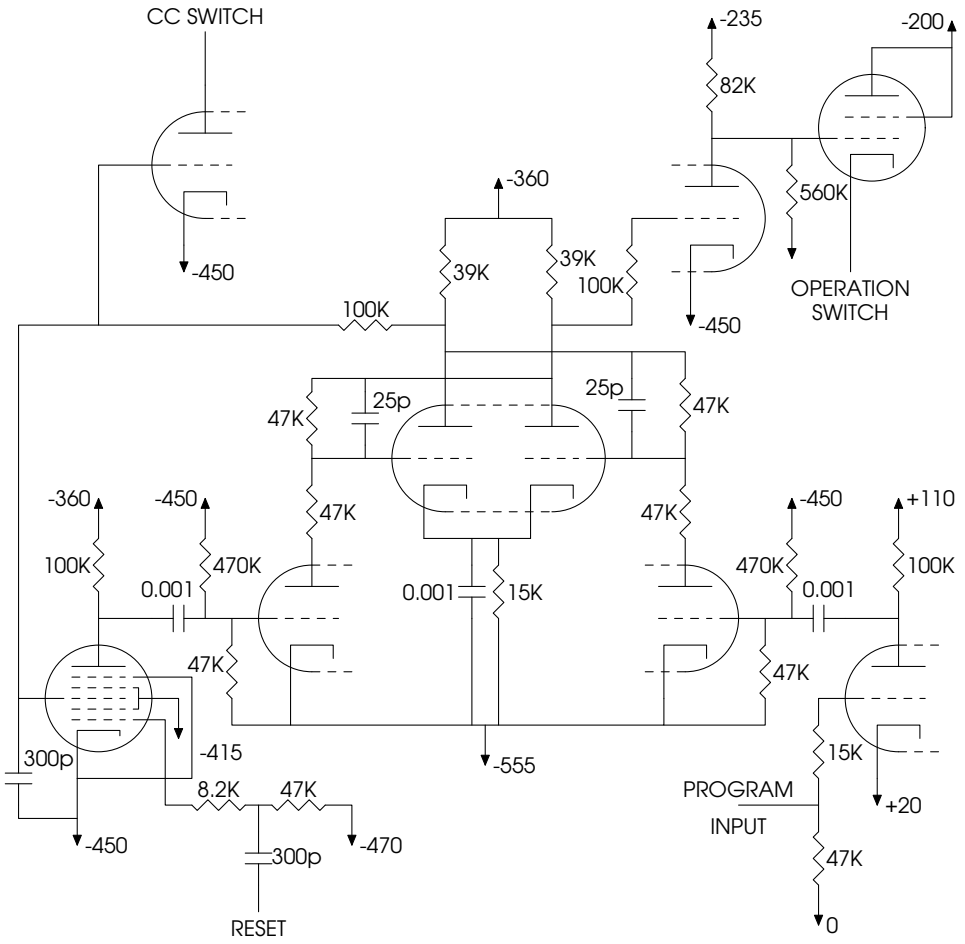

Figure 16. ENIAC Receiver

the next sub-paragraph. This signal also becomes one of the inputs, along with the CPP, to the second gate called the *transmitter gate.* The output of the transmitter gate becomes the reset signal for the transceiver flip-flop.

b. The transmitter gate also drives a standard transmitter circuit which gives the transceiver its name. This is ithe first of several differences between the outputs of a transceiver and those of a receiver. Two of the control outputs are handled the same in the receiver and transceiver. Both the buffer driving the program control switch and the buffer feeding the correction half of the CC switch come directly from the flip-flop state. The flop-flop output also controls a buffer that is ORed with the other transceivers to enable the CPP to drive the repeater counter. The remaining two outputs are generated by the repeat coincidence gate and feed the clear half of the CC switch and a signal to clear the repeater counter.

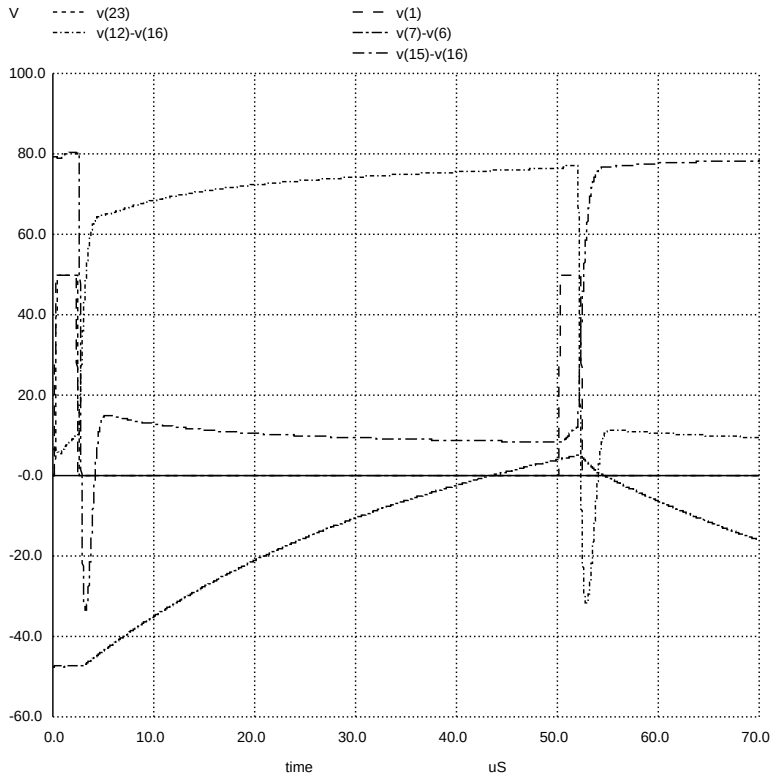

Figure 17. SPICE Simulation of Receiver

17. Accumulator Decade

The accumulator decade plug-in module is a large module containing 28 vacuum envelopes. Three envelopes are used for a pulse standardizer and driver, ten for a ten-stage ring counter, seven for the carry flip-flop and related gates, and eight for two transmitters and gates. The pulse standardizer, ring counter, and transmitters are discussed in earlier sections of this chapter. Operation of the carry circuits is discussed elsewhere along with the arithmetic aspects of the accumulator.

18. Accumulator PM and Clear

As one might guess from the name, the PM and Clear module handles two major functions in the accumulator. Ten of the tubes are 6L6s the drive the clear signals on the ten decade counters in the accumulator. The remainder of the module is a pulse standardizer, a two-stage counter, and two transmitters.

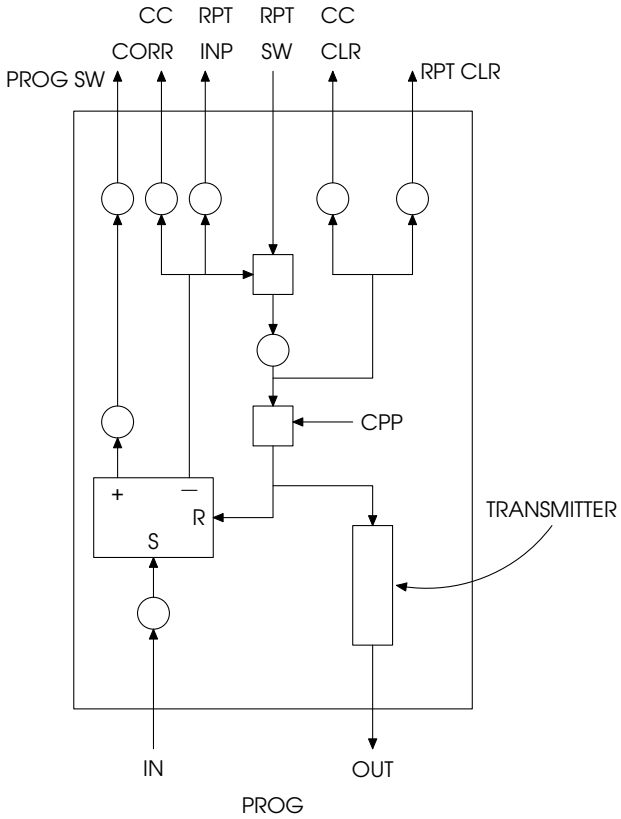

Figure 18. Transceiver Block Diagram