

SBUT_{1,2}

1	OUTPUT A1
2	A2
3	A3
4	A4
5	A5
6	A6
7	A7
8	A8
9	A9
10	A10
11	INPUT B
12	C
13	D
14	E

SG₁₋₆

1	REC'D TRAMP
2	PROG OUTPUT
3	REC'D IN Q1
4	PROGRAM IN
5	REP. CLEAR
6	STOP
7	PROG. HOLD
8	NOV. 1
9	CLEAR IN
10	-15V
11	CLEAR IN
12	REP. CLEAR

SAA₁₋₈

10	-25V
11	-315V
12	H4-1
13	-13C.H4-1

SK

1	PROGRAM IN
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	PULSE INPUT
12	REP. CLEAR

SL

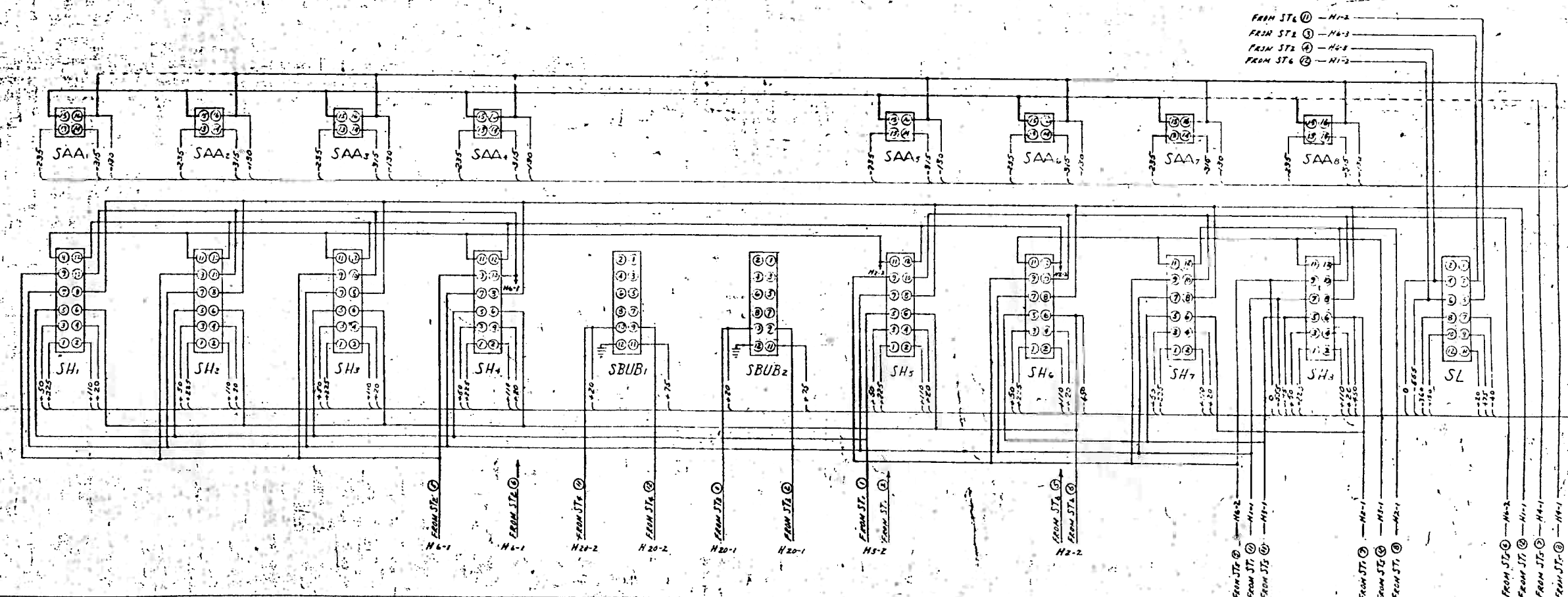
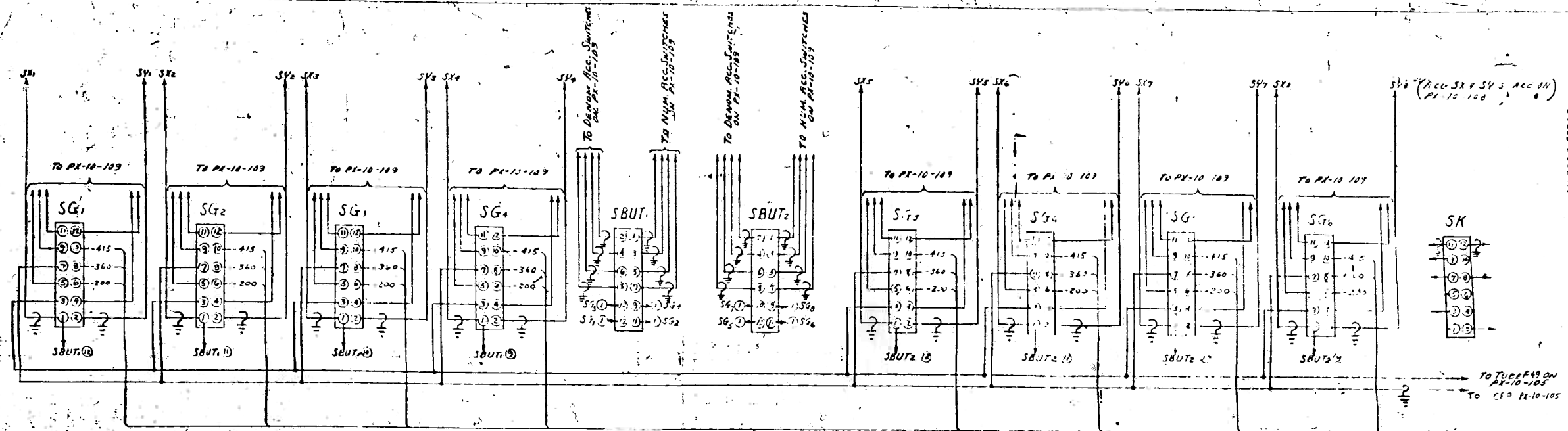
1	F
2	H4-2
3	H4-2 BDU
4	H4-2
5	H4-2 -33V
6	-40
7	-20
8	-20
9	-150
10	-20
11	-20
12	-20

SH₁₋₈

1	+225V
2	+110V
3	+25V
4	+25V
5	H3-2 H4-1
6	H3-2 H4-2
7	H4-1
8	H4-2
9	H4-2 H4-1
10	H4-2 H4-1
11	H3-2 H4-1
12	H3-2 H4-2

SBUB_{1,2}

1	
2	
3	
4	
5	
6	
7	
8	H20-2
9	H20-2 H20-1
10	H20-1
11	H20-1
12	SECURE



REVISIONS

1	SK WAS SRR. SL WAS SRT.
2	0 & 555 VOLTAGES ADDED ON SL.

MOORE SCHOOL OF ELECTRICAL ENGINEERING
UNIVERSITY OF PENNSYLVANIA

DIV. SOCKET PANEL #2

MATERIAL FINISH SCALE

Drawn by: *glp* 5/30/45
Checked by: *ether*
Approved by: *px-10-107*