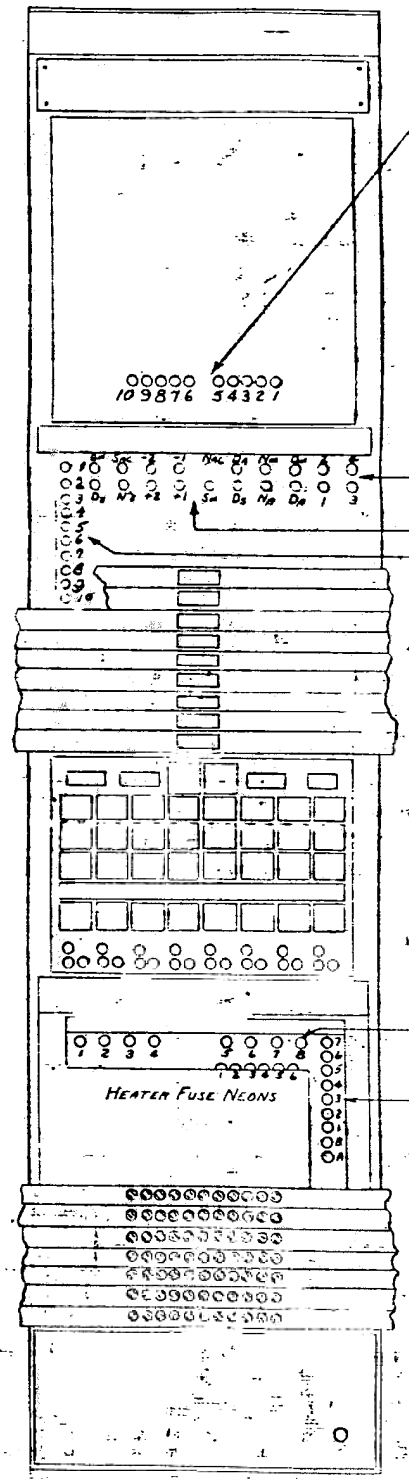


PERIOD	DIVIDE			ROOT		NEONS									
	STEPS (N-D+)	STEPS (N-D-)	PULSES	STEPS	PULSES	1	2	3	4	5	6	7	8	9	10
I INITIATING	Wait (receive arguments)	Wait (receive arguments)	GP,	Wait (receive arguments)	GP,										
	Wait (let PM lines set up)	Wait (let PM lines set up)	1'P,	Wait (let PM lines set up)	1'P,										
	Set numerator binary and denominator FF	Set numerator binary and denominator FF	DP	Set numerator binary and denominator FF	SRP										
II A	N_x, D_x	N_x, D_x		N_x, D_x											
	$Q_x, +1$	$Q_x, -1$		$D_x, +2$											
II B	$(D_x^*), N_{AC}, S_A$	$(D_x^*), N_{AC}, S_A$		$D_x^*, N_{AC}, S_A, -1$											
	Answer decade and numerator binary stepped.	Answer decade and numerator binary stepped.		$D_x^*, S_{AC}, N_x, -1$											
II A	N_x, D_A	N_x, D_x		N_x, D_A											
	$Q_x, -1$	$Q_x, +1$		$D_x, -2$											
II B	$(D_x^*), N_{AC}, S_A$	$(D_x^*), N_{AC}, S_A$		$D_x^*, N_{AC}, S_A, +1$											
	Answer decade and numerator binary stepped.	Answer decade and numerator binary stepped.		$D_x^*, S_{AC}, N_x, +1$											
II A	N_x, D_x	N_x, D_A		N_x, D_x											
	$Q_x, +1$	$Q_x, -1$		$D_x, +2$											
III ROUND OFF	$(D_x^*), N_{AC}, S$	$(D_x^*), N_{AC}, S$	III P,	$D_x, N_{AC}, S, -1$	III P,										
	Numerator binary stepped	Numerator binary stepped	[ROP]	Numerator binary stepped.	[ROP]										
	N_x, D_A	N_x, D_x		N_x, D_A											
	"	"		"											
	"	"		"											
	"	"		"											
	Wait for PM lines to set up	Wait for PM lines to set up		Wait for PM lines to set up											
	If no overdraft: $Q_x, +1$	If no overdraft: $Q_x, -1$		If no overdraft: $D_x, -2$											
IV INTER-LOCK	Wait for interlock input**	Wait for interlock input**	DP,	Wait for interlock input**	DP,										
	Set up clear circuits and transceiver gates	Set up clear circuits and transceiver gates	1'P,	Set up clear circuits and transceiver gates.	1'P,										
No OPERATION			GP, 1'P		SRP										



- NEON LAMPS (SEE ALSO PX-10-303)
1. DIVIDE FLIP-FLOP
 2. CLEAR FLIP-FLOP
 3. INTERLOCK FLIP-FLOP
 4. D_x RECEIVER
 5. N_x RECEIVER
 6. PULSE SOURCE FLIP-FLOP
 7. PROGRAM RING FLIP-FLOP
 8. DENOMINATOR FLIP-FLOP
 9. NUMERATOR RING
 10. NUMERATOR RING +

* BRACKETS MEAN THAT THIS IS DONE IF ROUND-OFF SWITCH IS SET TO ROUND-OFF; OTHERWISE TIME IS MARKED.
 ** ONE ADDITION TIME IS CONSUMED AT THIS STATION FOLLOWING THE ADDITION TIME DURING WHICH THE INTERLOCK PULSE IS RECEIVED.
 *** PULSES EMITTED FROM THE PULSE SOURCE CIRCUIT.

DRAWING REDRAWN FROM FRONT VIEW. NEONS ADDED.
 A. C. R. 12-12-45
 ARRANGEMENT OF NEON LAMPS CHANGED.
 C. A. R. 12-12-45
 NUMBERING OF TOP ROW OF NEONS REVERSED
 H. W. S. 12-12-45
 REVISION NUMBERING OF PULSE RING

MOORE SCHOOL OF ELECTRICAL ENGINEERING
 UNIVERSITY OF PENNSYLVANIA

DIVIDER & SQUARE ROOTER TIMING CHART

MATERIAL

Drawn by: C.J.M.C.
 Nov. 5, 1945

Checked by: [Signature]

Approved by: [Signature] PX-10-111