

TABLE 6-4
 DIVISION - INITIAL SEQUENCE - PERIOD I
 Requires three addition times: 1-3

Add. Time (and Prog. Ring stage)	Signal	Effect	Comment
0 (A)	1) Program input pulse	1) a) Sets transceiver in the divider b) Sets N_A or N_B and/or D_A or D_B receivers	1) a) b) The numerator and/or denominator are then received by the numerator and/or denominator accumulator respectively in <u>add. time 1.</u>
1 (A)	1) CPP	1) Gated through K_4^* by a signal from the pulse source flip-flop (in the normal state) produces a CP pulse.	1) This effect occurs in every subsequent add. time of a division program except during period III.
	2) GP	2) Gated through K_6 or L_6 produces a DP pulse.	2) This effect occurs in every subsequent add. time of a division program except during period III.
	3) DP	3) a) Gated through A_{10} by a signal from the program ring flip-flop, cycles the program ring to stage B. b) Sets the divide flip-flop if this flip-flop is in the normal state.	3) a) b) This turns on the divide flip-flop neon.
2 (B)	1) GP gated through D_6 by a signal from stage B of the program ring.	1) Is then gated through gate K_1 by the N^- signal so that the numerator binary ring is cycled to stage N in the event that the numerator is negative.	
	2) D^- signal	2) Is gated through D_1 by the output of gate 6. Output of gate D_1 sets the denominator flip-flop in the event that the denominator is negative.	2) This turns off the denominator flip-flop neon.
	3) DP	3) Cycles the program ring to stage 1	
3 (1)	1) DP	1) a) Gated through B_9 by a signal from stage 1 of the program ring produces a P pulse	
	2) P	2) a) Sets the N_Y receiver b) Gated through B_{10} when the like sign signal closes B_{11} sets the D_S receiver or gated through B_{11} when the unlike sign closes B_{10} sets the D_A receiver.	2) a and b) Then during <u>add. time 4</u> , the numerator accumulator receives either the complement of the denominator or the denominator. At the end of <u>add. time 4</u> , GP resets these receivers. The setting of these receivers is the event described (in the table for period II) as occurring in add. time $d=3+2n$ for $n=0$.
	3) GP	3) a) Gated through A_7 by a signal from stage 1, clears the program ring to stage A. b) Gated through B_7 flips the program ring flip-flop.	3) a) b) The program ring flip-flop neon is turned off at this time.

* \square refers to 'gate'.