

TABLE 6-6
 DIVISION PERIOD III - ROUND OFF OR NO ROUND OFF
 Items relevant only to the round-off case are circled
 Requires 9 add. times: 1-9

Add. Time	Signal	Effect	Comment
This add. time coincides with add. time d+2 of period II			
0 (A)	1) S pulse produced when a GP is gated through [E9] as a result of the coincidence of an 0 signal and a signal from the 2_a receiver. 2) SS pulse	1) a) Sets the S_a and N_{AC} receivers. b) Sets the D'_y receiver. c) Gated through [E6] as a result of the coincidence of signals from the places switch and place ring, produces an SS pulse. 2) Sets the pulse source flip-flop.	1) a) During add. time 1, then, the numerator accumulator transmits (and clears) its contents to the shift accumulator. A CPP resets these receivers in add. time 1. b) Since during add. time 1, there is no numerical data on the tray from which the D_y channel receives, there is no numerical result from 1 b). 2) At this time, the pulse source flip-flop noon is turned off.
1 (A)	1) CPP 2) III P	1) a) Gated through [I1] by a signal from the S_a receiver, cycles the numerator binary ring. b) Gated through [K7] by a signal from the S_a receiver, sets the S_{AC} and N'_y receivers. c) Gated by [E5] produces a III P pulse. 2) a) Gated by [K5] produces ROP. b) Cycles the program ring to stage B c) Resets the D'_y receiver.	1) a) So that NO ceases to be emitted and 0 is emitted by the sign indicating circuit. b) So that, during add. time 2, the numerator accumulator receives the number transmitted (with clearing) from the shift accumulator. At the end of add. time 2, these receivers are reset by a CPP. c) This pulse is produced in every subsequent add. time of period III. 2) ROP is produced in every subsequent add. time of period III if round off is specified.
2 (B)	1) III P 2) ROP 3) P	1) Cycles program ring to stage 1. 2) Gated through [E3] by a signal from stage B of the program ring, produces a P pulse. 3) Sets N_y and D_x or D_y receiver depending on whether the sign is like sign signal is emitted.	1) These receivers remain set during add. times 3, 4, 5, 6, and 7. (See below) They are reset at the end of add. time 7. Before the numerator accumulator receives either the number 1 or or its complement five times.
3 (1)	1) III P	1) Cycles program ring to stage 2	
4 (2)	1) III P	1) Cycles program ring to stage 3	
5 (3)	1) III P	1) Cycles program ring to stage 4	
6 (4)	1) III P	1) Cycles program ring to stage 5	
7 (5)	1) ROP 2) III P	1) Gated through [L2] by a signal from stage 5 of the program ring, resets the N_y and D_x or D_y receivers. 2) Cycles the program ring to stage 6.	
8	1) ROP 2) III P	1) Gated through [M3] by a signal from stage 6 of the program ring, produces a signal which, if gated through [N3] by NO, passes through [O3] to set the 2_a receiver and through [P3]. The signal from [Q3] passes through [R3] when the like sign signal is emitted and sets the +1 receiver or passes through [S3] to set the -1 receiver when the unlike sign signal is emitted. 2) Cycles the program ring to stage 7.	1) Thus, if the subtraction or addition of 5 times the denominator which takes place during add. times 5 through 7 does not produce an overdraft, during add. time 8 the quotient is increased (was numerator and denominator have like signs) or decreased (when numerator and denominator have unlike signs) by 1 unit in the last place at the right as specified by the setting of the places switch. At the end of add. time 8, III P resets and the +1 or -1 receiver, and a CPP resets the 2_a receiver.