

TABLE 6-7
 SQUARE ROOT PERIOD I
 Requires four add. times: 1-4

Add. Time (and Prog. Ring Stage)	Signal	Effect	Comment
0 (A)	1) Program input pulse	1) a) Sets transceiver in the divider and square rooter. b) Sets N_0 or N_0 receiver	1) b) The numerator is then received by the numerator accumulator during add. time 1.
1 (B)	1) CPP	1) Gated through K_4 by a signal from the pulse source flip-flop, produces a GP pulse.	1) This effect occurs in every subsequent add. time of a square root program except during period III.
	2) OP	2) Gated through L_3 or K_3 produces a SRP	2) This effect occurs in every subsequent add. time of a square root program except during period III.
	3) SRP	3) a) Gated through A_{11} by a signal from the program ring flip-flop, cycles the program ring to stage B. b) Resets the divide flip-flop if this flip-flop is in the abnormal state.	3) b) This turns off the divide flip-flop neon.
2 (1)	1) GP gated through D_6 by a signal from stage B of the program ring.	1) Gated through K_1 by the N^- signal cycles the numerator ring to stage E if the radicand is negative.	1) The divider and square rooter, however, does not find the real coefficient of i correctly if the radicand is negative.
	2) SRP	2) Cycles the program ring to stage 1.	
3 (A)	1) SRP	1) a) Gated through K_8 by a signal from stage 1 of the program ring, sets the D_y receiver. b) Gated through G_7 by a signal from stage 1 of the program ring, sets the +1 receiver.	1) a and b) Thus, during add. time 4, the denominator (twice the root) accumulator receives 1 pulse in the 10^8 decade. At the end of add. time 4, a CPP resets the D_y receiver and a GFP gated through as a result of the coincidence of the N_0 signal and a signal from the D_y receiver, resets the +1 receiver.
	2) OP	2) a) Gated through A_7 by a signal from stage 1, clears the program ring to stage A. b) Gated through R_7 by a signal from stage 1 flips the program ring flip-flop.	2) b) The program ring flip-flop neon is turned off at this time.

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