

TABLE 6-8
 SQUARE ROOT PERIOD II - BASIC SQUARE ROOT SEQUENCE
 Requires two add. times; r+1, r+2

Add. Time	Signal	Effect	Comment
		For n=0, this add. time coincides with add. time 4 of period I. For n>0, this add. time coincides with add. time s+2 or r+2 of period II.	
r (=4+2n for n>0) (A)	1) P pulse derived from GP gated through [D9] as the result of the coincidence of a signal from the D _Y receiver and an NO signal or GP gated through [C9] by a signal from the N _Y receiver (after a shift sequence).	1) a) Sets the N _Y receiver. b) Gated through [B10] when the like sign signal is emitted, sets the D _S receiver or gated through [B11] when the unlike sign signal is emitted, sets the D _A receiver.	1) a and b) Thus, during add. time r+1, the numerator accumulator receives the complement of the denominator (when N and D have like signs) or receives the denominator (when N and D have unlike signs). These receivers are reset by GP at the end of add. time r+1.
r+1 (A)	1) SRP	1) a) Gated through [L9] by a signal from the N _Y receiver sets the D _Y receiver. b) Gated through [G12] or [H12] respectively by a signal from the D _S or D _A receiver sets the +2 or -2 receiver.	1) a and b) Thus, in add. time r+2, the denominator accumulator receives two in a given decade place of the complement of 2 if the denominator was previously subtracted or added respectively. The D _Y receiver and the +2 and -2 receivers are reset by a CPP at the end of add. time r+2.

SQUARE ROOT - SHIFT SEQUENCE

Requires two addition times: s+1, s+2

Add. Time	Signal	Effect	Comment
		This add. time coincides with add. time r+2	
s (=4+2n for n>1 - (A)	1) S pulse produced when a GP is gated through [E9] as a result of the coincidence of an 0 signal and a signal from the D _Y receiver.	1) a) Sets the S _A and N _{AC} receivers. b) Sets the D _Y receiver. c) Gated through [G9] by a signal from the +2 receiver, sets the -1 receiver or gated through [H9] by a signal from the -2 receiver, sets the +1 receiver. d) If gated through [E6] as a result of the coincidence of signals from the places switch and places ring produces an SS pulse (see Table 6-9).	1) a) As a result, the shift accumulator receives the numerator from the numerator accumulator which transmits and clears during add. time s+1. At the end of add. time s+1, a CPP resets these receivers. b and c) During add. time s+1, then, the denominator accumulator receives the complement of 1 or receives 1 in a given decade place if during the previous sequence, the denominator accumulator received +2 or -2 respectively in the same decade place. The D _Y receiver and the +1 or -1 receiver remain set through add. time s+2. d) SS pulse initiates period III. (See chart for period III.)
s+1 (A)	1) Signal from the S _A receiver.	1) a) Gates 1 ^o P ₁ through [L45] to produce 1 ^o P ₂ which cycles the place ring one stage. b) Gates a CPP through [L1] so that the numerator binary ring is cycled 1 stage. c) Gates a CPP through K7 so that the N _Y and S _{AC} receivers are set.	1) b) As a result 0 ceases to be emitted and NO is emitted instead. c) During add. time s+2, then, the numerator accumulator receives the contents of the shift accumulator which transmits and clears. At the end of add. time s+2, a CPP resets the N _Y and S _{AC} receivers. 2) Therefore, during add. time s+2, the denominator accumulator receives +1 or the complement of 1 but this time one decade place further to the right than during add. time s+1. At the end of add. time s+2, GP gated through [C11] by a signal from the N _Y receiver resets the D _Y receiver and the +1 or -1 receiver.
	2) See 1 c) of addition time s.	2) The D _Y and +1 or -1 receiver remains set.	