

TABLE 6-9  
 SQUARE ROOT PERIOD III - ROUND OFF OR NO ROUND OFF PERIOD  
 Requires nine add. times; 1-9  
 Items relevant to the round off case only are circled

Add. Time	Signal	Effect	Comment
This add. time coincides with add. time r+2 of period II.			
0 (A)	1) S pulse produced when a CP is gated through <u>E9</u> as a result of the coincidence of an 0 signal and a signal from the Q <sub>a</sub> receiver.	1) a) Sets the S <sub>a</sub> and N <sub>AC</sub> receivers.  b) Sets the D' <sub>γ</sub> receiver.  c) Gated through <u>G9</u> by a signal from the +2 receiver, sets the -1 receiver or gated through <u>H9</u> by a signal from the -2 receiver sets the +1 receiver.  d) Gated through <u>E6</u> as a result of the coincidence of signals from the places switch and place ring produces an SS pulse.	1) a) <u>During add. time 1</u> , then, the numerator accumulator transmits (and clears) its contents to the shift accumulator. A CPP resets these accumulators in <u>add. time 1</u> . b and c) Thus, <u>during add. time 2</u> , the denominator accumulator receives the complement of -1 or +1 in a given decade place if in the previous square root sequence, +2 or its complement respectively was received in that decade place. At the <u>end of add. time 1</u> , III P (see below) resets the D' <sub>γ</sub> and +1 or -1 receivers.
	2) SS	2) Sets the pulse source flip-flop.	2) At this time, the pulse source flip-flop neon is turned off.
1 (A)	1) CPP	1) a) Gated through <u>L1</u> by a signal from the S <sub>a</sub> receiver cycles the numerator binary ring. b) Gated through <u>K7</u> by a signal from the S <sub>a</sub> receiver, sets the S <sub>AC</sub> and N' <sub>γ</sub> receivers.  c) Gated by <u>F6</u> produces a III P.	1) a) So that NO ceases to be emitted and 0 is emitted instead. b) So that <u>during add. time 2</u> , the numerator accumulator receives the numerator from the shift accumulator which transmits and clears. At the <u>end of add. time 2</u> , a JII resets these receivers. c) This pulse is produced in every subsequent add. time of period III.
	2) III P	2) a) Gated by X4 produces an ROP pulse. b) Cycles the program ring to stage B. c) Resets the D' <sub>γ</sub> receiver and the +1 or -1 receiver.	2) a) ROP is produced in every subsequent add. time of period III if round off is specified.
2 (B)	1) III P	1) Cycles program ring to stage 1	1)
	2) ROP	2) Gated through <u>C8</u> by a signal from stage B of the program ring produces a P pulse.	2)
	3) P	3) Sets N <sub>γ</sub> receiver and D <sub>A</sub> or D <sub>S</sub> receiver if the unlike or like sign signal respectively is emitted.	3) These receivers remain set <u>during add. times 3,4,5,6,7</u> . They are reset at the <u>end of add. time 7</u> (see below). Therefore, the numerator accumulator receives either the denominator or its complement five times.
3 (1)	1) III P	1) Cycles program ring to stage 2.	
4 (2)	1) III P	1) Cycles program ring to stage 3.	
5 (3)	1) III P	1) Cycles program ring to stage 4.	
6 (4)	1) III P	1) Cycles program ring to stage 5.	
7 (5)	1) ROP	1) Gated through <u>D4</u> by a signal from stage 5 of this program ring resets the N <sub>γ</sub> and D <sub>A</sub> or D <sub>S</sub> receivers.	
	2) III P	2) Cycles the program ring to stage 6.	
8 (6)	1) ROP	1) Gated through <u>J13</u> by a signal from stage 6 of the program ring produces a signal which if gated through <u>K12</u> by NO, passes through <u>J9</u> to set the D <sub>γ</sub> receiver and passes through <u>J12</u> . The signal from <u>J12</u> passes through <u>E13</u> when the like sign is emitted and sets the +2 receiver or passes through <u>F13</u> when the unlike sign signal is emitted and sets the -2 receiver.	1) Thus, if the subtraction or addition of 5 times the denominator which occurs <u>during add. times 3 through 7</u> does not produce an overdraft, <u>during add. time 9</u> , the quotient is increased (when N and D have like signs) or decreased (when N and D have unlike signs) by 2 units in the last place at the right as specified by the setting of the places switch. At the <u>end of add. time 9</u> , III P resets the +1 or -1 receiver and a CPP resets the D <sub>γ</sub> receiver.