

TABLE 6-10
 PERIOD IV FOR EITHER DIVISION OR SQUARE ROOT - INTERLOCK OR NO INTERLOCK PERIOD
 Requires 2 add. times: 1, 2.
 Items relevant to the interlock case only are circled.

Add. Time	Signal	Effect	Comment
This add. time coincides with add. time 9 or period III			
0 (7)	1) CPP	1) Gated through <u>L50</u> by a signal from stage 7, or the program ring, produces an F pulse. b) Gated through <u>E3</u> by a signal from stage 7 or the program ring produces an F pulse.	1) This turns on the interlock coincidence flip-flop neon. 2) So that the pulse source flip-flop neon is turned on again.
	2) F	2) Sets the interlock coincidence flip-flop.	
	3) F'	3) Resets the pulse source flip-flop.	
1 (7)	1) CPP	1) Gated through <u>P4</u> produces a CP.	These three pulses continue to be produced every add. time of period IV but have no effect on the division or square rooting. 4) The clear flip-flop neon goes on at this time and the interlock coincidence flip-flop neon goes off.
	2) CP	2) Gated through <u>K6</u> or <u>L6</u> produces a DP or through <u>K3</u> or <u>L3</u> produces a SRP.	
	3) 1'P	3) Gated through <u>F6</u> produces 1'P ₁ .	
	4) CPP	4) Gated through <u>K49</u> in the NI case or (gated through <u>J49</u> in the I' case) produces a signal which is gated through <u>H50</u> to set the clear flip-flop and to reset the interlock coincidence flip-flop.	
2 (7)	1) CPP	1) Gated through <u>F49</u> by a signal from the clear flip-flop, produces a CL' pulse.	e) Thus, during the add. time following the divider's program output pulse, the answer is disposed of in accordance with the setting of the answer disposal switch. At the end of add. time 3, the answer disposal receiver is reset by a CPP.
	2) CL'	2) Gated through <u>L48</u> by a signal from the interlock switch, resets the interlock flip-flop. b) Clears the program ring to stage A. a) After passing through buffer <u>E48</u> becomes a CL pulse.	
	3) CL	3) Resets the clear flip-flop. b) Clears the numerator binary ring to stage P. c) Resets the denominator flip-flop. d) Clears the place ring to stage 1. e) Resets the program ring flip-flop.	
	4) Signal resulting from the coincidence of the transceiver's being set and the clear flip-flop's being set.	4) Allows the carry clear gate to pass to the numerator and/or denominator accumulator clear circuits if clearing is specified. b) Gates a CPP through <u>G8</u> to provide a reset signal for the transceiver and a program output pulse. c) Gates a CPP to set one of the four answer disposal receivers.	

*If the interlock input pulse is not received until k addition times after add. time 0 of period IV, this event and all events listed next to add. time 2 occur k addition times later than that indicated in this table.