



**CODE**

	Gate lead		Input terminals
	Buffer or inverter		Output terminals
	Pulse standard cap.		Input digit plug
	Transformer		Output digit plug
	Flip-Flop (S-Set R-Reset)		Interconnecting terminals (front panel, see PA-5-300)
	Resistor plug-in unit		Pulse
	Ring counter		CCG Carry-Clear-Gate
	Gate lead		CPP Control Program Pulse
	Pulse lead		ICG Input Clear Gate
	Cable lead		RP Reset Pulse
	Cable lead		A Add
	Cable lead		S Subtract

Decade cap. and other "S" circuits and static outputs.

SCHOOL OF ELECTRICAL ENGINEERING  
UNIVERSITY OF PENNSYLVANIA  
**REGULATOR BLOCK DIAGRAM**

FINISH \_\_\_\_\_ SCALE \_\_\_\_\_

Drawn by \_\_\_\_\_  
Checked by \_\_\_\_\_  
Approved by \_\_\_\_\_

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PLAINTIFF'S TRIAL EXHIBIT  
No. 3238