

TABLE 5-4

CHRONOLOGICAL OPERATION OF HIGH SPEED MULTIPLIER'S PROGRAMMING CIRCUITS

Note: It is assumed here that ten-decade accumulators are used for the partial products.

Add. Time for 2 digit multiplier	Stage of Ring Counter	In High Speed Multiplier's programming circuits	In associated accumulators
End of Add. time 0	1	1) Program input pulse is received and re-transmitted to ier and/or icand accumulators	1) See addition time 1.*
1	1	1) Ring cycles to stage 2 at CPP time.	*Ier and icand accumulators receive arguments.
2	2	1) 1P passed by B ⁴⁷ sets l and r receivers. 2) 1 ^r P gated through A ⁴⁷ and 4P through A ⁴⁶ are delivered to round off gates. 3) Ring cycles to stage 3.	1) LHPP and RHPP accumulators' receive on α circuits are activated. 2) LHPP accumulator receives five round-off pulses.
3	3	1) Signal from stage 3 opens ier selector K gates so that multiplier tables are entered with first from the left ier digit. 2) Signal from stage 3 opens A ^r shifter gates. 3) Ring cycles to stage 4.	1 and 2) LHPP accumulator receives tens digits of "icand x first ier digit" in decade places 10 through 1. RHPP accumulator receives units digits of "icand x first ier digit" in decade places 9 through 1.
4	4	1) Signal from stage 4 opens ier selector J gates and shifter B ^r gates. 2) Signal from B ⁴⁶ gates a 1 ^r P through L ⁴⁷ . 3) Signal from B ⁴⁶ gates CPP through B ⁴⁶ to initiate RS and DS corrections if R and/or D are negative. 4) Signal from B ⁴⁶ gates CPP through B ⁴⁸ to provide reset signal for l and r receivers. 5) Signal from B ⁴⁶ allows CPP to pass through F ⁴⁶ to clear ring to stage 13.	1) LHPP accumulator receives tens digits of second P.P. in decade places 9 through 1. RHPP accumulator receives units digits of second P.P. in decade places 8 through 1. 2) PH counter of RHPP accumulator receives 1 ^r P if both ier and icand are L.S.D. 3) See addition time 5.** 4) LHPP and RHPP accumulators' receive on α circuits cease to be activated.
5	13	1) Signal from stage 13 allows CPP to pass through M ⁴⁹ and K ⁵⁰ to the reset flip-flops for program controls 1-8 and 17-24. 2) Signal from stage 13 gates a CPP through A ⁴⁷ so that P pulse is emitted 3) Ring cycles to stage 14.	**RS and/or DS corrections are made (see addition time 4). 2) See addition time 6.***
6	14	1) Signal from stage 14 goes to reset gates of program controls 9-16 to reset these controls. All other program controls are reset by signals from reset flip-flops. 2) Ieand and ier accumulator clear signals are emitted. 3) Program output pulse and product disposal signal are emitted. 4) Ring cycles to stage 1.	***LHPP and RHPP are combined. 2) Argument accumulators clear.
7	1		Product is transmitted from final product accumulator.