TABLE 2-2 - INITIAL CLEARING OF ENIAC UNITS

UNIT	ITEM	MANNER OF INITIAL CLEARING OR RESETTING
Accumulator	Flip-flops in receivers and transceivers.	No provision for direct reset of receivers or transceivers. However, if a F.F. comes up in the abnormal state, the program set up on the associated switches is carried out and, in a maximum of 9 add. times, the F.F. is reset.
	Decade flip-flops	Normally negative output of decade F.F. gates RP through gate 18 so that a decade F.F. in abnormal state is reset.
	Repeater ring	CPP gated through K50 by ICG resets repeater ring.
	Decade counters and FM counter	CCG gated through L44 by ICG clears counters.
Multiplier	Flip-flops in transceivers	Reset in maximum of 14 add. times (see Accumulator).
	Program ring	If program ring is not in stage 1, CPP is gated through J'44. ICG holds G'44 open so that output of J'44 is passed to prog. ring. Thus the ring is cycled to stage 1. When prog. ring is in stage 1, J'44 is closed so that no other CPP are admitted to cycle the ring.
	Reset flip-flops	Normally negative output of a reset F.F. which comes up in abnormal state opens G49 or L'50 so that a CPP is passed to reset the F.F..
	L and R receivers	ICG gates CPP through E'47 to reset these receivers.
	Ra-R8, Da-D8, and answer disposal receivers	Reset by CPP.
Divider and Square Rooter	AT PRESENT, ICG gates a CPP through E50. The output of E50 gives rise to CL and CL' pulses so that clearing is accomplished as follows:	
	Flip-flops in transceivers	No provision for direct reset, since the reset signal from transceivers in the divider comes from the clear F.F. and the present method of init. cl. does not ensure that the clear F.F. will be set during init. cl. Since a divider program may last longer than init. cl. finishing a program cannot be depended on for resetting program controls in this unit.
	Program ring	Cleared to stage A by CL' signal.
	Pulse source flip-flop	Reset by CL'.
	D'_γ, +2, and -1 receivers	Reset by CL'.
	Program ring flip-flop	Reset by CL.
	Numerator Binary Ring	Cleared to stage P by CL.
	Denominator flip-flop	Reset by CL.
	Answer Place Ring	Cleared to stage 1 by CL.
	Clear flip-flop	Reset by CL.
	Interlock flip-flop	Reset by CL' gated through K48 by ICG.
	Interlock coincidence flip-flop	NOT RESET by the present method.
	S_{AC}, H'_γ, S_{Ca}, H_{AC}, D_γ, Q_{Ca}, +2, -2 answer disposal and argument accumulator receivers.	Reset by CPP.
	H_γ, D_Δ, D_β	Reset by CP emitted after pulse source flip-flop is reset.
	It is planned to modify the design of the divider in such a way that the interlock coincidence F.F. will be eliminated and also so that the transceivers will be reset during the init. cl. period.	
Function Table	Flip-flops in transceivers	Reset in a maximum of 13 add. times (see Accumulator).
	Argument flip-flop and Add. and Sub. flip-flops	Reset by CPP gated through C48 by ICG.
	Program ring	Cleared to stage -3 by CPP gated through B48 held open by ICG.
	Units and tens argument counters	Cleared by CPP gated through A48 by ICG.
Constant Transmitter	Flip-flops in transceivers	Reset in 1 add. time (see Accumulator).
Reader	Start flip-flop	Reset by CPP gated through 63 by ICG.
	Interlock flip-flop Finish flip-flop Synchronizing flip-flop	Reset by CPP gated through 71 by ICG.
Printer	Start flip-flop	Reset by CPP gated through 71 by ICG.
	Finish F.F. is set by CPP gated through 71 by ICG. Then CEP gated through 66 sets synchronizing F.F. Normally negative output of synchronizing F.F. gates CPP through 69 so that: Finishing and Synchronizing flip-flops are reset by the output of gate 69.	
Master Programmer	MPC holds stepper output gates closed so that master programmer cannot emit a program output pulse.	
	Stepper input flip-flops	Reset by CPP gated through 69 if F.F. is in abnormal state.
	Stepper Counters	Cleared to stage 1 by CPP gated through C47 by ICG.
	Master programmer decade counters	Cleared to stage 0 by CPP gated through B44 by ICG.

Under the present method of initial clearing, a card may be fed to the reader or punch in the period between the turning on of the power and the resetting of the start flip-flop.